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A Review on SRAM Memory Design Using FinFET Technology

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ABSTRACT

An innovative technology named FinFET (fin field effect transistor) has been developed to offer better transistor circuit design and to compensate the necessity of superior storage system (SS). As gate loses control over the channel, CMOS devices face some major issues like increase in manufacturing cost, less reliability and yield, increase of ON current, short channel effects (SCEs), increase in leakage currents, etc. However, it is necessary for the memory to have less power dissipation, short access time, and low leakage current. The traditional design of SRAM (static RAM) using CMOS technology represents severe performance degradation due to its higher power dissipation and leakage current. Thus, a nano-scaled device named FinFET is introduced for designing SRAM since it has three-dimensional design of the gate. FinFET has been used to improve the overall performance and has been chosen as a transistor of choice because it is not affected by SCEs. In this work, the researchers have reviewed various FinFET-based SRAM cells, performance metrics, and the comparison over different technologies.

KEYWORDS

CMOS, FinFET, Short Channel Effect, SRAM, Static Noise Margin

INTRODUCTION

For a long time, the integration procedure used by the researchers is the VLSI (Very Large Scale Integration). The process in which millions of transistors are integrated into a single chip, thereby creating an IC (Integrated Circuit) is termed as VLSI. The advancements in the field of VLSI, brings rise of innovative technologies which further enhance the speed of circuit and also minimize the design constraints. Electronic gadgets have moved to the trend of miniaturization. Today, all the Smart Gadgets (SG) are introduced in small, portable and compact sizes. The most common circuits present in these devices are the memory and processor. For most of the designs, the need for memory is increasing nowadays. In today's development, beyond 85-90% of the chip area is occupied mainly by memory. The two memory devices namely Static Random Access Memory (SRAM) and Dynamic random-access memory (DRAM) provides significant performance for SSD (Solid State Drives). A solid-state drive (SSD) is a solid-state storage device that uses integrated circuit assemblies to store data persistently, typically using flash memory, and functioning as secondary storage in the hierarchy of computer storage. However, there is a necessity for reliable as well as quicker memory for different

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integrated devices. SRAM (Agrawal & Tomar, 2018; Pasandi et al., 2019) plays a significant role which offers low-power and high-performance for VLSI applications. Reliability issues give rise to leakage problems, process variations and SCEs which occur as a result of rapid scaling in CMOS (Complementary Metal Oxide Semiconductor) (Juneja et al., 2021) design. SRAM is faster, reliable and consume less power (Chiu et al., 2012) however, affected by means of CMOS scaling (Mocuta et al., 2018; Yusop et al., 2018) triggering process variations. CMOS size shrinking makes the scaling of dimensions possible which further results in stability and power issues. In CMOS devices, the main problem is scaling of supply voltage causes threshold voltage scaling. Due to Moore's law, the CMOS scaling is transformed into nano-scale system (Zhang, 2018). Therefore, CMOS scaling has now come to a limit with the following possible alternatives such as FinFETs (Ensan et al., 2019), TFET (Tunnel FET) (Galli, 2020), and CNTs (Carbon Nano Tubes) (Jia & Wei, 2019). Among these alternatives, FinFET technology (Birla, 2019; Panda, 2019) is chosen as the best option for replacing CMOS. FinFET provides several advantages over bulk CMOS, for instance higher speed, higher drive current for a given transistor footprint, lower leakage, no random dopant fluctuation, lower power consumption, better mobility and transistor scaling. Several low power techniques named Variable Threshold CMOS (VTCMOS), Multi-threshold CMOS (MTCMOS), Stacking technique, Self Controllable Voltage Level (SVL), Power gating are also used to minimize the leakage current and power dissipation. Initially, SRAM is designed using traditional CMOS. However, this creates some problems like increase in leakage current and high power dissipation which disturbs the SRAM performance. It is essential for the memories to have low leakage current, shorter access time and less power dissipation. So, FinFET based SRAM cells are suggested over CMOS based SRAM cells (Panchal & Ramola, 2017). SCEs are minimized using FinFET design when compared to CMOS based design structures (Narendar & Mishra, 2015). Also, to improve the cell stability it is essential to shrink the leakage characteristics of SRAM cells (Majhi, 2018).

Rest of this review paper is organized as follows. Section 2 defines about FinFET technology and SRAM architecture. The objective is mentioned in Section 3. The various FinFET-SRAM cells are explained in Section 4. The evaluation metrics are mentioned in Section 5. Next, Section 6 describes the analytical results of FinFET and SRAM under different technologies. Section 7 represents the comparison of various related works. Finally, Section 8 is the conclusion followed by references.

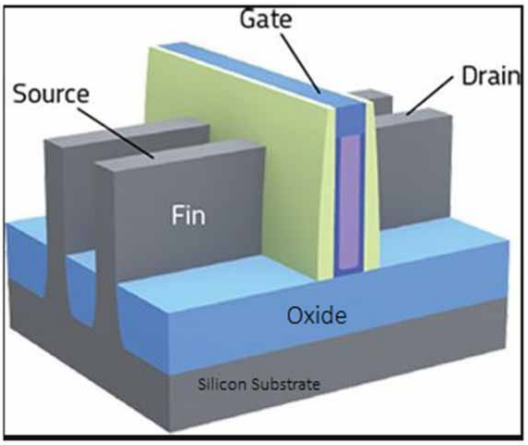
BACKGROUND

This section presents the basic concepts and related terminologies about FinFET and SRAM memory architecture.

- **FinFET Technology:** In today's era, one of the most suitable forms of FET is FinFET technology (Jurczak et al., 2009). This permits the execution and simulation of transistor applications in a faster way both in analog as well as digital domains. FinFET seem to be a better option for the future nano electronics because of its following characteristics such as compact susceptibility, high performance, minimized manufacturing costs and low power consumption (Dadoria et al., 2017; Guo et al., 2016). The bulk CMOS transistors can be replaced by means of FinFETs (Yakimets et al., 2017). This technology is an appropriate option for the design of memory sub-systems due to its standby power or low leakage current property (Garg & Singh, 2016).

The diagrammatic representation of FinFET is mentioned in Figure 1. The FinFET structure includes multiple perpendicular channels that appear similar to 'Fin' of fish, so it is named as FinFET. It is also known as Multi-Gate Device (MGD) which is built on a substrate. The gate is positioned on two, three or else four sides of the channel which forms a double gate arrangement. The source or drain region forms 'Fin' on the surface of silicon. The other name of FinFET is multi-gate transistor. The FinFET model includes the following regions:

Figure 1. Structure of FinFET



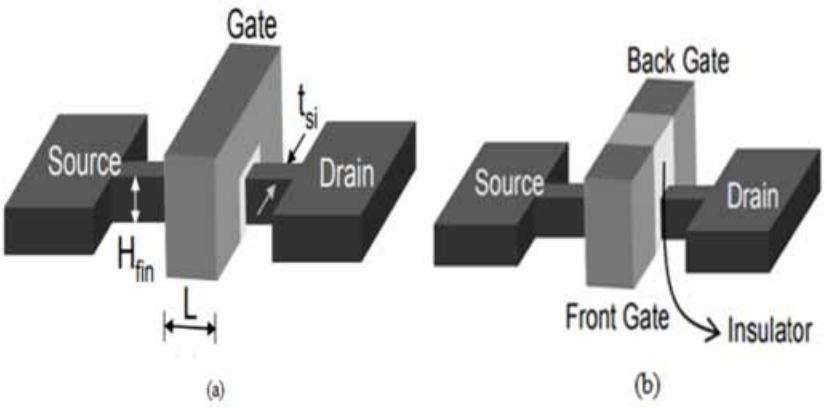
- **Gate-oxide region (SiO2):** Highly doped poly-silicon region.
- **Low doping silicon Fin:** Highly doped contact region between source and drain.

FinFET transistors can operate on dual model namely Tied-gate (TG) and Independent-gate (IG) mode (Girish, 2015). The 3D representation of FinFET- TG and IG mode is shown in Figure 2.

In TG-mode, both of the Front as well as Back Gates (FBGs) are tied to the similar Control Signal (CS). The design of TG-FinFET is simpler with shorted FBG. The SCEs are avoided by the TG-mode because this mode has greater gate-to-channel coupling. IG-FinFET combines the P-type parallel FinFET and tie with the BGs of N-type to ground in order to attain equivalent rising as well as falling delays. Both the FBGs are tied to different control signals in the IG-mode. FinFET devices ensure higher current density and faster switching times than the CMOS technology. Also, by minimizing the off-state leakage the SCEs are controlled.

Various design options are offered by the FinFET structures. It works on various modes such as IG, TG, hybrid and low power mode. The combination of both IG and low power mode is known as hybrid mode (Rajprabu et al., 2013). FinFET devices are similar to CMOS device from the view of Fabrication. But, FinFET offers superior performance gains at very low power due to higher gate

Figure 2. (a) TG FinFET 3D-view (b) IG FinFET 3D-view



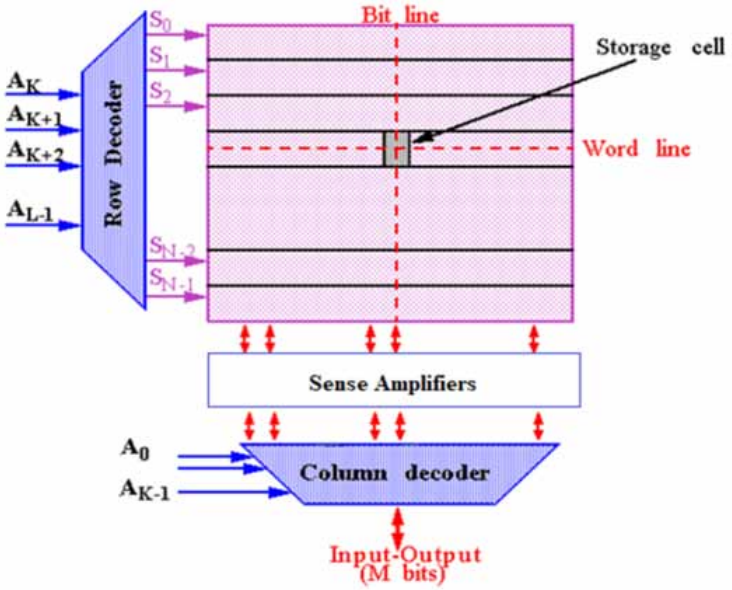
control. To suppress the SCEs, gate-dielectric leakage currents the FinFET devices are used. FinFET is a favourable technique to bridge the technology gap between bulk CMOS and other novel devices, such as CNTFETs and Graphene FETs. Thus, FinFET technology is introduced as a new procedure for designing an SRAM cell with ultra-low leakage. Also, it advances the characteristics of SRAM cell in write, read, and in hold mode. Some of the advantages of FinFETs are: Insensitive to channel doping, Improved Matching and exceptional SCE control, Higher Gain and Low cost, More compact and better in driving current, Scaling density beyond planar devices (sub 20nm), Large effective channel width, Lower threshold and source-drain leakage, Scalability and Higher technological maturity than planar DG (Double-Gate) transistors.

- **SRAM Memory:** Static RAM is a kind of RAM that holds data in static form, until the memory has power. There is no need of periodic refreshing in SRAM. Since it is volatile in nature, the data gets lost if it is not powered. SRAM make use of bi-stable latching circuitry in order to store each bit. SRAM is used in internal CPU caches, workstations, PCs, and hard disk buffers etc. The array architecture of SRAM memory is shown in Figure 3.

The structure of SRAM array includes the following: Bit line, Sense amplifier, Word line, Row and Column decoder and Storage cell. Numerous words are stored in a single row and are selected simultaneously. Address word is divided into row and column addresses. To perform read or else write operation, only one row of memory is enabled by the row address whereas the column address selects one from the selected row. The storage cell is otherwise named as 1-bit memory cell or bit-cell which includes a latch circuit (2-cross coupled inverters) with dual main operating states. The data present in the storage cell can be represented as logic '1' or '0'. SRAM cell consists of 3 different operational states: Standby or Hold (Circuit is idle), Read (Request for data) and Write (contents updating).

SRAM memory cell normally consists of simple cross-coupled inverters that are connected back to back, and two access transistors (Tiwari et al., 2017). Whenever a word line (WL) is activated for read or write operation, the access transistors are turned ON connecting the cell to the complementary bit line (BL) columns. The most important advantage of this circuit topology is that the static power

Figure 3. Architecture of SRAM memory



dissipation is very small, medium power consumption, small leakage current and need less time to access data (Bhaskar, 2017; Gavaskar & Ragupathy, 2017).

OBJECTIVE

The main purpose of this work is to review the various SRAM memory design using FinFET technology. Some of the unique features of FinFET are work function engineering, mobility, corner effect, and volume inversion. FinFET based design structure offers improved performance, reduced cost and greater circuit functionality.

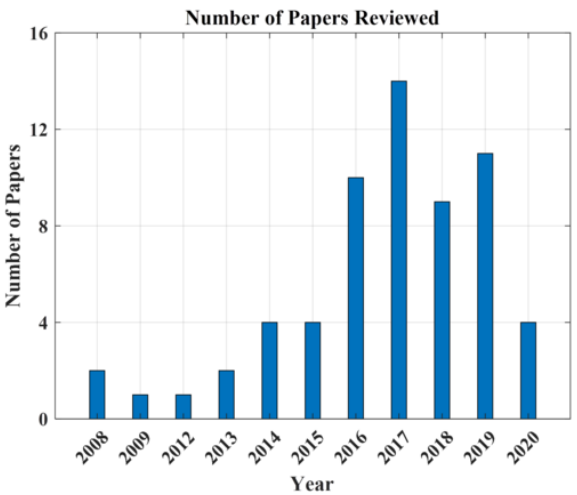
- **Choice of sources:** The choice of data starts by setting practical screening norms in order to make sure that only qualified publications are used in the review. In this survey, only the papers, reports, survey articles, editorial notes which are written in English is used and other languages are excluded. Eventually, 62 articles are considered for analysis. The important characteristics desirable for the selection procedure defines the indexed article exposure (belongs to magazines or else journals), study accessibility, and methods. Table 1 show the names of 4 search engines (SEs) used for the source selection. In this survey, the papers from 2008 to 2020 are chosen and the sources are taken from the SEs such as Wiley online library, IEEE, Springer and Elsevier.

Figure 4 signifies the graphical review of particular sources used from the following years. This graph displays the assessment of number of papers from the year 2008 to 2020.

Table 1. SE selection

Names of SE	Link
Wiley online library	https://onlinelibrary.wiley.com/
IEEE Explore	https://ieeexplore.ieee.org/
Springer	https://link.springer.com/
Elsevier	https://www.elsevier.com/

Figure 4. Review of certain sources



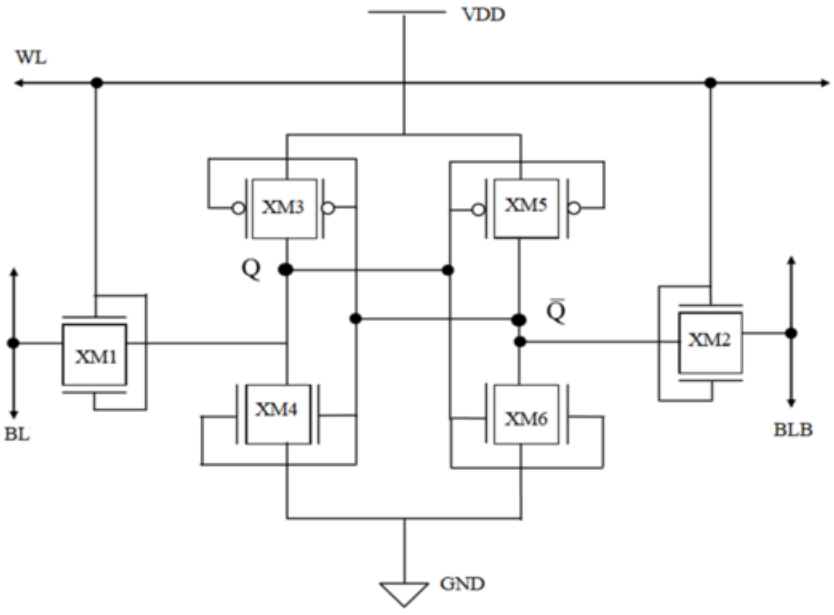
FinFET Based SRAM Cells

Advanced circuit methodology is essential to bridge the gap between power, area, robustness, frequency and quality in cases of maintaining the abundant manufacturing outcome. FinFET based structures are introduced as an alternate to bulk devices. Several methods have been implemented earlier, mainly to reduce the static power dissipation. However, these devices can only be able to decrease the leakage current variations. Thus, to boost the cell stability and to minimalize the leakage power various FinFET based SRAM cells are introduced.

- **FinFET-6T SRAM cell:** The 6T (6Transistor) SRAM (Limachia & Kothari, 2020) includes two cross-coupled (2-CC) inverters and dual access FinFET transistors. The 2-CC inverters consist of 4 transistors named as (XM3, XM4, XM5 and XM6). In SRAM, each bit is stored on these 4 FinFET transistors. The two access FinFETs are (XM1, XM2) and the source terminals are linked to BL and BLB (BLBar). 6T SRAM cell is widely used basic cell as it occupies smaller area. The dual access FinFETs are enabled when WL=1 and the bit lines are connected to latch which performs read or else write operation. When WL=0, the access transistors move to OFF state and BL, BLB are separated from the latch. The schematic diagram of FinFET based SRAM 6T cell is presented in Figure 5.

The three fundamental operations are read, write and hold (Banu & Shubham, 2017; Gupta et al., 2017). In hold mode, WL is attached to ground (GND). Hence the transistors XM5 and XM6 become OFF and separate the latching circuit from the bit lines. The remaining transistors (XM1, XM2, XM3 and XM4) forms a latch structure which holds a stored data until it is disconnected from the bit lines. During read mode, pre-charge the bit lines to VDD also WL is attached to VDD and the transistors XM5 and XM6 becomes ON. The transistors XM1 and XM4 are in OFF state if Q=1 and $\bar{Q}$ =0 and XM3 and XM2 becomes ON. Hence, the voltage level of BL sustains at VDD and BLB voltage level discharges. At write mode, WL is attached to VDD and makes the transistor XM5 and

Figure 5 FinFET 6T- SRAM CELL



XM6 ON. Then the node voltage level $\bar{Q}$ starts to rise up to the voltage level at which Q is ample to turn ON the transistors XM4 and XM2 and Q get drops.

- **FinFET-7T SRAM cell:** The representation of 7T-FinFET SRAM cell is mentioned in Figure 6. The 7T (7Transistor) cell design (Asli & Taghipour, 2017; Sneha et al., 2017) includes 2-CC inverters namely (XM3, XM4, XM5, and XM6) with an additional transistor (XM7) that is linked to the WL. Also, dual access transistors (XM1, XM2) are attached with the BL and BLB respectively. The leakage problem occurred in the 6T cell is solved using 7T FinFET structure. To execute the read as well as write processes, the XM1 and XM2 transistors are attached to WL. During read and write operation, the dual bit lines serve as input or else output nodes, in order to detect the data from SRM cells using sense amplifier.

The working procedure defines that at hold mode, the WL is turned OFF and the transistors XM3 and XM4 become inactive. Due to logic 0 in SRAM cell, a sub-threshold leakage current flows via the transistors in OFF state. And the supplementary transistor XM7 performs feedback connection as well as disconnection and the SRAM cell depends only on the BLB to execute write operation (Ansari et al., 2015; Yang et al., 2016).

- **FinFET-8T SRAM cell:** The 8T (8Transistor) (Neelima et al., 2020) FinFET SRAM cell is introduced to overcome the limitations of 6T cell. The main problem is that the read and writes procedures are not decoupled. The cell with lower SNM (Static Noise Margin) during read mode possibly has enhanced write ability. Therefore, if the read, write functions are decoupled perfectly, the circuit designers have superior flexibility in optimizing read and write functions. The schematic representation of FinFET-8T SRAM cell is shown in Figure 7.

The 8T design is introduced to separate the read operation from write in order to attain improved stability when allowing low-voltage operations (Guler & Jha, 2019; Neelima et al., 2020). The 8T configuration represents that, addition of 2 FETs to a 6T cell offers a read processes which won't

Figure 6. 7T- FinFET SRAM CELL

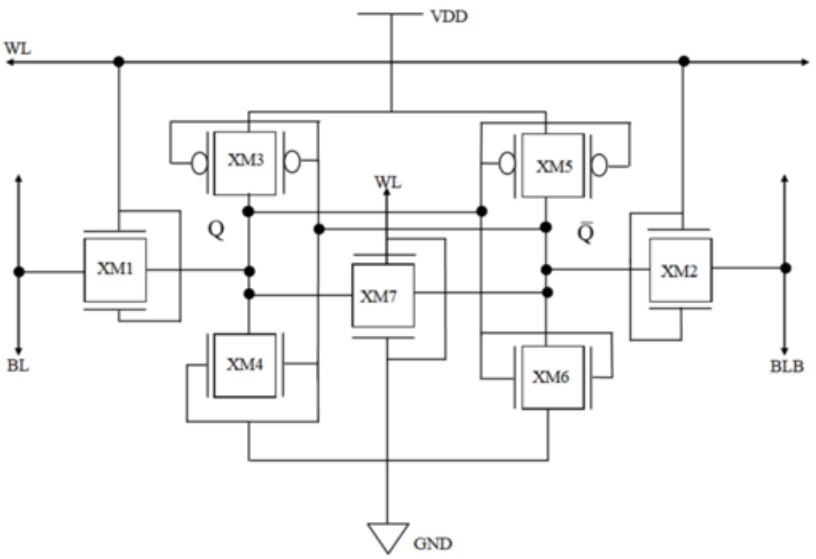
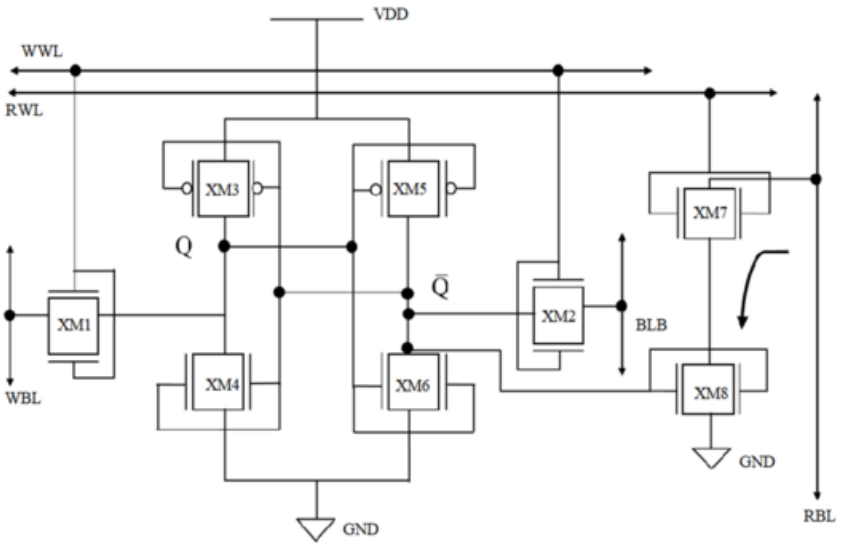


Figure 7. FinFET 8T- SRAM CELL



interrupts the internal nodes of cell. Hence, this process needs Separate Read Word Line (RWL) and Write Word Line (WWL). Read mode operation is done by activating RWL and pre-charging RBL. The XM6 transistor turns ON if 1 gets stored at Q and creates a low resistance path for the cell current flow via RBL to GND detected by sense amplifier (Alias et al., 2019; Monica & Chandramohan, 2017).

- **FinFET-9T SRAM cell:** The 9T (9Transistor) FINFET SRAM cell mainly includes dual sub-sections (Moradi & Tohidi, 2015; Oh et al., 2016; Sharma, 2016; Yatimi & Aroudam, 2018). The upper section of 9T SRAM is similar to 6T cell design composed of (XM1, XM2, XM3, XM4, and Q & $\bar{Q}$). This primary sub-section is utilized to store data. The other section in 9T SRAM includes dual (XM5 and XM6) bit-line access transistors and one read access transistor (XM9). The operations of transistors (XM8 and XM7) depends on the data stored in the cell. XM9 depends on the separate read signal (RD). The write access transistors perform write access which is controlled by WBL and WBLB (write bit lines). Also, read access transistor executes read access which is controlled using RWL (Read word line). The schematic representation of 9T FinFET SRAM cell is mentioned in Figure 8.

9T cell design is introduced to solve the leakage problem identified on the 8T cell RBL. This causes change in data during read processes. 8T cell is limited to low-density applications that can be solved using 9T structure (Adding XM9 transistor in between XM7 and XM8). Therefore, leakage in BL is reduced significantly by the stack effect phenomena. In 9T SRAM, when OFF state transistors are connected in series, stacking takes place. Thus, the upper transistor source voltage will be somewhat higher than lower transistor source voltage in stack. The threshold voltage is increased due to higher voltage of the upper transistor. This increment of the threshold voltage reduces the leakage. Hence, this reduction is called stack effect.

- **FinFET-10T SRAM cell:** The 10T (10Transistor) SRAM cell includes 4 pull-up, 4 pull-down and 2 access transistors. The design of 10T cell using FINFET is shown in Figure 9. In order to minimize the power dissipation and leakage current, this 10T cell is introduced. The deployment of dual threshold-voltage technique is performed using the transistors in read path, which

Figure 8. 9T- FinFET SRAM CELL

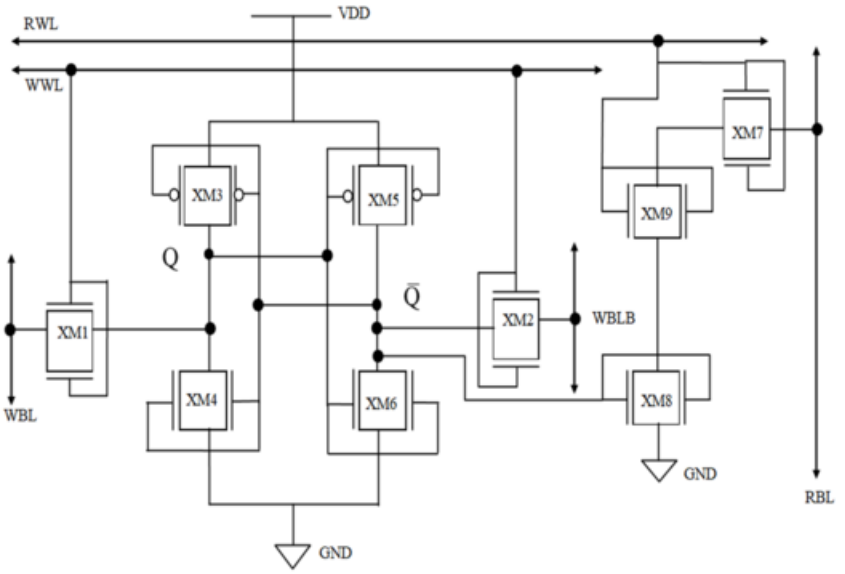
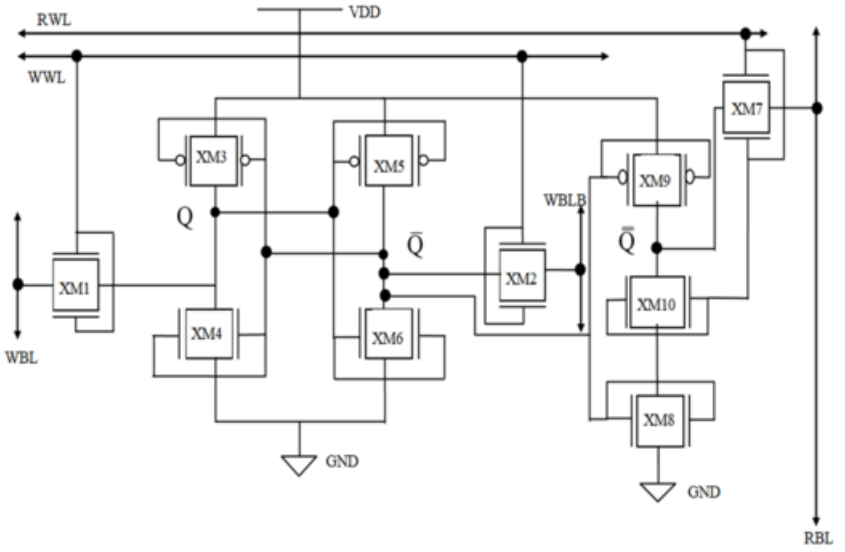


Figure 9. 10T- FinFET SRAM CELL



enhances the current ON or else OFF ratio. The source of XM10 and gate of XM9 transistors are attached to RWL. Also, WWL, BL, BLB are linked to the access FinFETs. The write margin is improved by means of transistors XM7 and XM8. Here, the static current is minimized using access transistors new size assumption which is twice the size of pull-up transistors. Apart from access transistors, all the other transistors used in the design of 10T are fixed to a minimum possible gate length (Chiranjeevi & Jena, 2017; Ichihashi et al., 2018; Kaur et al., 2016; Singh et al., 2019; Yadav et al., 2013).

FinFET based 10T design, minimize the leakage current using transistors (XM7, XM8, XM9 and XM10) when compared to 9T cell design. For read operation, the two access transistors are used to connect the pseudo nodes. The read stability is maintained well, as there is no flow of read current by storage nodes. To perform write operation, the node Q stores I value whereas $\bar{Q}$ stores 0. By applying a high supply voltage, the node Q is pulled down to '0' due to discharging through the access and the pull-up transistor.

- **FinFET-11T SRAM cell:** The 11T (11Transistor) SRAM is designed to improve the energy consumption. One of the main challenges in SRAM design is static power consumption. This 11T design focuses on minimizing the static power consumption and improving the performance at sub-threshold region. The transistors XM2, XM4, XM5 and XM6 perform the similar characteristics as that of 6T SRAM cell. Also, the transistors (XM2, XM3) size is scaled down equivalent to the p-MOS transistor size. The 11T cell includes WL, BL, RWL and separate read, write ports (Karri & Jena, 2016; Maabi et al., 2016).

The schematic representation of FinFET 11T SRAM cell is shown in Figure 10. This cell attains low power dissipation due to its series connected drivers driven by BL, BLB and read buffers.

- **FinFET-12T SRAM cell:** The 12T (12Transistor) FinFET SRAM cell includes the following transistors such as XM3, XM7, XM4, XM5, XM8 and XM6, and differential Read or else Write ports, XM9, XM1, XM11, XM10, XM2 and XM12. Write Word-Line 1 (WWL1), WWL2, BL, and BLB are column-based whereas RWL and VGND (Virtual Ground) are row-based. The reduction in current and power validates 12T design approach (Rokbani et al., 2020; Yadav et al., 2017).

Figure 10. 11T- FinFET SRAM CELL

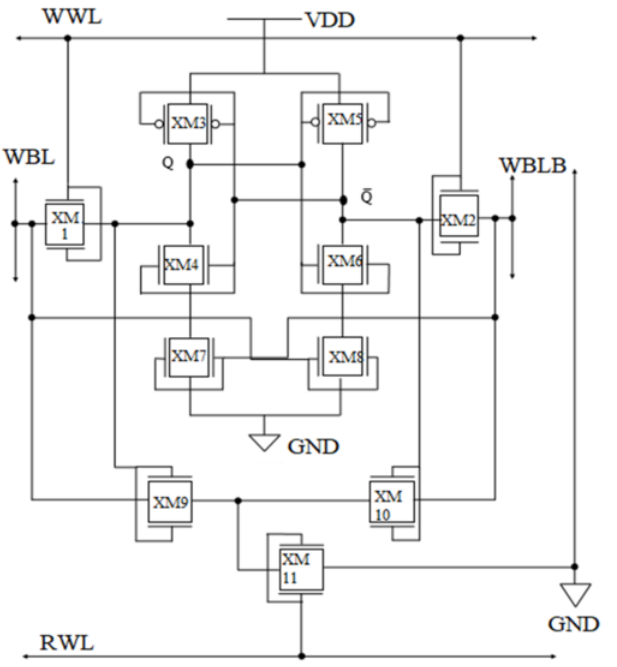


Figure 11 illustrates the schematic representation of 12T SRAM. This 12T bit-cell is intended for low-voltage operation. Internally the bit-cell cuts off supply voltage for either the left or right half-cell to weaken the pull-up network of the bit-cell during write operation. This structure advances write-ability without using extra peripheral write assist circuits, related boosting and timing control circuits.

- **FinFET-13T SRAM cell:** SRAM cell stability is decreased by means of the following fluctuation effects of intrinsic parameter. Some of them are random dopant variation, line-edge roughness and variation in gate-oxide-thickness. 13T SRAM cell is designed to attain higher SM and better performance. The processes such as read (R) and write (W) are separated in most of these cells to attain greater NM. The 13T (13Transistor) structure (Saxena & Mehra, 2016) includes CC Schmitt trigger (ST) inverter, dual transistors in read path, and one MAL (write-access transistor) which is controlled by row-based WL, and MAR1 (read-access transistor) is controlled by row-based RWL. The ST13T SRAM cell includes design variation in the proposed representation with the transmission gate (TG) usage in access path. TG moves over the entire voltage range, i.e. strong '0' and strong '1' which increases the device performance. FinFETs provide improvements in power and energy consumption since they overcome the leakage problems of planar devices and deliver better performance (Guo & Stan, 2020).

PERFORMANCE METRICS

This section describes the FinFET based SRAM cell performance metrics. Some of the common metrics used to evaluate the performance of FinFET structures are as follows:

- **Static Noise Margin (SNM):** The standard metric which is used to measure the SRAM bit-cell stability is known as SNM. It depends on the cell ratio (CR), supply voltage and also pull up ratio (PR). Good SNM is required for the stability of SRAM cell. During read process, the ratio between sizes of driver transistor to the load transistor is named as CR. At, write operation the ratio between sizes of load transistor to the access transistor is termed as PR. SNM is also known as butterfly method. The representation of SNM or butterfly curve is mentioned in Figure 12.

Figure 11. 12T- FinFET SRAM CELL

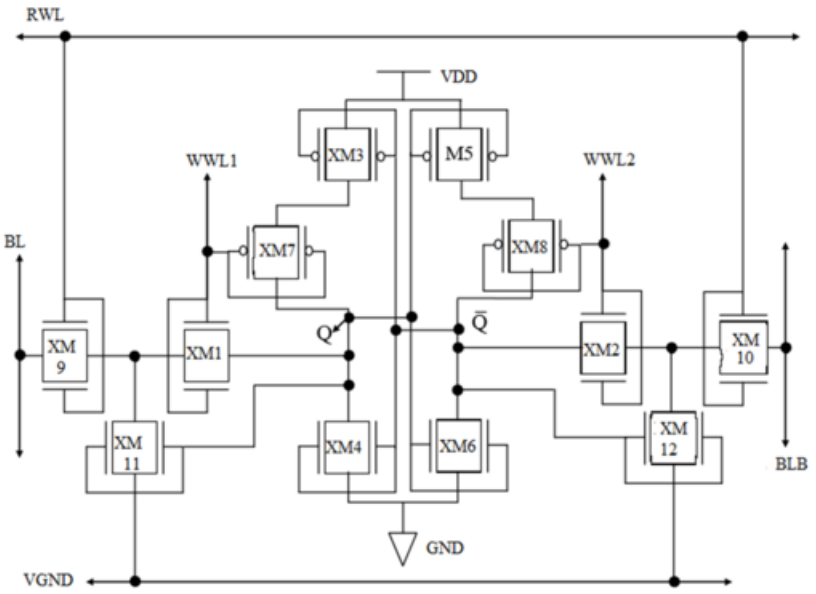
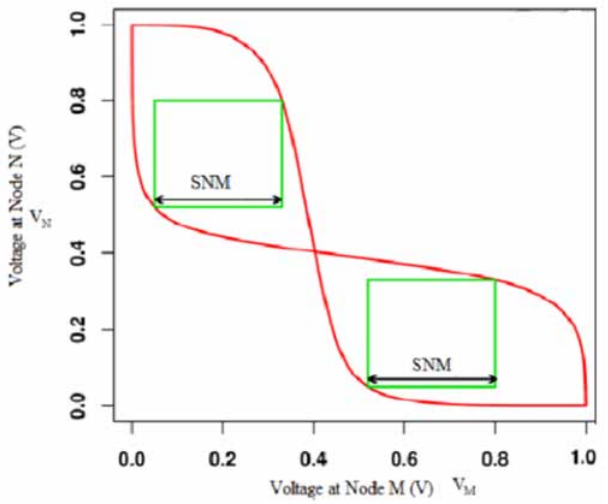


Figure 12. SNM representation



For 70% value of the SNM, the Driver transistor (DT) is responsible. Both read as well as write margin, is affected by means of SNM which is interrelated to the threshold voltages (THV) of the NMOS and PMOS devices in SRAM cells. Varying CR offers different speed of SRAM cell. If CR increases, then size of the DT also increases, whereas current also rises. As the current starts to increase, speed of SRAM cell also increases. By varying the CR value SNM is acquired. For different values of CR, we got diverse SNM in different technology of SRAM cell.

- **Read Noise Margin (Read NM or RNM):** The SRAM cell robustness is measured using RNM. Read NM is directly proportional to CR. The pull-down FinFET should be higher than access transistors, in order to obtain higher RNM. Pull-up ratio depends on the transistor size. Therefore, RNM increases with increase in pull-up ratio value. Also, read margin is directly proportional to CR. The analysis of RNM procedure is similar to that of SNM. Read NM is defined to characterize the read ability of SRAM cell based on the voltage transfer curves (VTCs). The transistor's current model is used to measure RNM. Read NM is improved by pull-down transistor upsizing which further results in increasing the access FinFET gate length. A cautious FET device is essential to evade writing 1 accidentally in SRAM cell. CR determines how high the "0" storage node rises during a read access. Smaller CRs translate into a bigger voltage drop across the pull FinFET requiring a smaller noise voltage at the "0" node to trip the cell.
- **Write Noise Margin (WNM or Write NM):** WNM is used to write data into SRAM cell. The maximum bit line voltage which is able to flip the FinFET –SRAM cell state when BLB voltage is kept high is known as WNM. Write NM is directly proportionate to pull-up ratio. Therefore, WNM increases with increase in pull-up ratio value. The maximum noise voltage (NV) present at bit lines (BLs) during successful write operation is called as WNM voltage. Write failure occurs only if the When NVs exceeds the WNM voltage. Higher the Write NM, greater is the stability. The use of access FinFET and weaker pull-up helps to store 1 to quicker discharge therefore facilitate a faster write 0. Thus, Write NM enhances with strong access and weak pull-up FinFET at the cell read margin.
- **Power and Delay:** FinFET-SRAM cell PDi assesses the utility of cell in portable devices. The major benefit of SRAM using FinFET technology is low access time as well as small power dissipation. PD (propagation delay) is mainly influenced by column height in addition to wire delays in SRAM. Therefore delay is minimized by segmentation procedure. As the PDP (power-

delay-product) is constant for a device, then upsizing FinFET device decreases the delay with a little increased PDi. In order to decrease PDi, leakage currents required to be decreased with an increase in channel length (CL) or else higher transistor THV.

- **Temperature:** This is an important metric, as the increase in temperature affects the performance of the device while it is turned ON or else OFF. Power dissipation (PDi) often leads to increase in device temperature. The local temperature rise can create circuit failure and can also influence power, performance and reliability. Temperature may have a considerable effect on other design parameters such as access time. With increase in temperature, the leakage current increases exponentially and hence, the power dissipation increases substantially in FinFET device. Hence, temperature is one of the most important performances metric in future VLSI circuit designs.

POWER DELAY PRODUCT (PDP)

PDP is measured by transient analysis performance of SRAM cells. It is a metric for energy consumption of a circuit. The product of gate delay and the average power defines PDP. Moreover, PDP favours the processor that operates at lower frequency. An efficient SRAM cell should have lower PDP for read and write operations. The size of transistor is set is attain minimum PDP by optimizing the transistor size which further minimize the delay without increasing the power consumption.

ANALYSIS OF SRAM FINFETS USING VARIOUS TECHNOLOGIES

This section describes the analysis for the various SRAM cell at different nm (nanometer) technology.

Table 2 shows the performance analysis of 6T SRAM in 22 nm technology (Banu & Shubham, 2017) and the tool used is Predictive technology model library. Table 3 denotes the 6T SRAM comparison in CMOS and FinFET technology (Chiranjeevi & Jena, 2018). Table 4 represents the comparative performance of 6T SRAM in Planar and FinFET technology (Kumar & Chalil, 2019) in Hspice. Table 5 denotes the comparison of 7T with other SRAM cells (Sneha et al., 2017) and the simulation tool used is Tanner. The Table 6 indicates the comparative analysis of 7T SRAM (Garg & Singh, 2016) in H-spice tool. Table 7 shows the Comparison of FinFET 7T and 8T SRAM (Kushwah & Akashe, 2014) using Cadence Virtuoso Tool. Table 8 indicates the Comparison of 9T FinFET at different technologies (Vijapur & Uma, 2018) in Cadence software. Table 9 shows the comparison of 10T and 6T FinFET at 7-nm technology (Mushtaq & Sharma, 2020) in Cadence Virtuoso tool. Table 10 represents the comparison of 11T FinFET SRAM with other cells in 10-nm technology (Ensan et al., 2018). Table 11 denotes the 12T FinFET SRAM comparison in 32-nm technology (Rokbani et al., 2020) with HSPICE simulator. Table 12 depicts the 13T FinFET SRAM comparison in 22-nm technology (Saxena & Mehra, 2016) using Cadence Virtuoso Tool (V.6.1).

- **Comparison of Various Finfet Based Sram Cells:** From Table 13, comparison of different FINFET-SRAM cell is analysed based on its technology, device name, technique used and special features. Table 13 represents the FinFET based SRAM comparison.

Table 2. Performance analysis of 6T SRAM in 22 nm technology (Banu & Shubham, 2017)

Type/ Parameter	Technology	Write delay (ps)	Read delay (ps)	Write power (nW)	Read power (nW)	SNM (mV)	Temperature (°C)
Conventional 6T SRAM	22 nm	112	947	243	746	240	25
FinFET 6T SRAM	22 nm	98	610	1.6	1.98	280	25

Table 3. Comparison of 6T SRAM in CMOS and FinFET technology (Chiranjeevi & Jena, 2018)

CMOS (45-16nm)								
Technology/ Parameter	L(nm)	W(nm)	T_{OX}(nm)		V_{th0}HP		V_{th0}LSTP	
			HP	LSTP	NMOS	PMOS	NMOS	PMOS
45 nm	45	90	1.25	1.8	0.46	-0.49158	0.6226	-0.587
32 nm	32	64	1.15	1.6	0.49	-0.49155	0.63	-0.5808
16 nm	16	32	0.95	1.2	0.47	-0.43121	0.68191	-0.6862
FinFET (16-7nm)								
Technology/ Parameter	L(nm)	W_{FIN}(nm)	H_{FIN}(nm)		WF HP		WF LSTP	
					NFET	PFET	NFET	PFET
16 nm	20	12	26		4.41	4.76	4.58	4.59
7 nm	11	6.5	18		4.42	4.74	4.61	4.56

Table 4. Comparative analysis of 6T SRAM in Planar and FinFET technology (Kumar & Chalil, 2019)

Temp (°C)	Planar (MOSFET) Technology					FinFET Technology				
	SNM (mV)	Write margin (mV)	Read current (A)	Leakage current (A)	Cell standby leakage current (A)	SNM (mV)	Write margin (mV)	Read current (A)	Leakage current (A)	Cell standby leakage current (A)
-40	165.17	274.43	2.32E-05	4.46E-11	1.55E-11	192.74	302.43	1.25E-04	3.04E-11	1.49E-11
27	156.12	266.21	2.24E-05	1.15E-09	4.41E-09	184.23	292.31	1.18E-04	2.35E-10	1.02E-09
40	156.07	265.11	2.23E-05	2.07E-09	6.99E-09	184.20	292.02	1.17E-04	3.59E-10	4.00E-09
125	129.15	242.43	19E-05	4.37E-09	9.81E-09	175.57	276.63	1.10E-04	7.02E-10	6.22E-09

Table 5. Comparison of 7T with other SRAM cells (Sneha et al., 2017)

Parameters	Technology	6T FinFET(Tied)	6T FinFET INDE	7T SRAM-Bit line replaced	7T SRAM Bit line replaced and NMOS stack	8T SRAM
Power dissipation(watts)	45 nm	1.358e-006	5.648e-007	1.280e-007	6.702e-008	4.684e-007
Delay (sec)	45 nm	6.948e-010	1.733e-009	1.280e-007	6.702e-008	6.29e-010

Table 6. Comparative analysis of 7T SRAM (Garg & Singh, 2016)

Technology/Parameter	Average power (μW)	Delay (ns)	Power Delay Product (fj)
CMOS (22nm)	0.169	0.129	0.0219
CMOS (16nm)	0.139	0.223	0.0311
FinFET (22nm)	0.023	0.090	0.0021
FinFET (16nm)	0.015	0.002	0.0028

Table 7. Comparison of FinFET 7T and 8T SRAM (Kushwah & Akashe, 2014)

Parameters/SRAM cell	CMOS		FINFET	
	7T	8T	7T	8T
Leakage current	14.12 μA	34.67 μA	3.094 nA	55.56 nA
Leakage power	26.34 μW	35.87 μW	38.10 nW	60.90 nW

Table 8. Comparison of 9T FinFET at different technologies (Vijapur & Uma, 2018)

Parameter/ Type	SPNM μW	Write Access(ps)		WTP μW	Leakage power μW	Read power(nW)		Write power(nW)		Read Access(ps)	
		0	1			0	1	0	1	0	1
9T (180nm)	7.55	82.52	119.5	-7.31	3.26	162.3	63.8	110.2	89.5	20.44	15.35
9T (7nm)	7.53	14.67	78.51	-11.7	0.804	48	53.9	15.41	56.32	15.83	7.2

Table 9. Comparison of 10T and 6T FinFET at 7-nm technology (Mushtaq & Sharma, 2020)

Parameter/ Type	Leakage power μW		Propagation Delay (psec)		PDP (aJ)		SNM (mV)	
	Read	Write	Read	Write	Read	Write	Read	Write
6T FinFET	10.68	31.01	12.8	13.98	136.8	433	124.45	195
10T INDEP FinFET	7.26	26.5	18.01	16.10	129.6	426.6	106.06	309.7

Table 10. Comparison of 11T FinFET SRAM with other cells in 10-nm technology (Ensan et al., 2018)

Type/ Parameters	SNM (mV)		Delay (ps)		Average power (nW)	Static power (nW)	PDP(aJ)
	Read	Write	Read	Write			
7T	70	198	491.8	230.46	194.95	4.76	128.28
8T	183	80	640.26	1749.2	226.72	6.85	701.38
9T	183	225	676.61	275.09	631.17	4.37	445.54
11T	175	225	676.17	218.27	137.66	5.17	168.57

Table 11. 12T FinFET SRAM comparison in 32-nm technology (Rokbani et al., 2020)

Type/Parameter	Average power		
	HOLD (nW)	READ (nW)	WRITE (nW)
12T (CMOS)	180.79	161.30	201.61
12T (FinFET)	14.06	45.64	60.06

Table 12. 13T FinFET SRAM comparison in 22-nm technology (Saxena & Mehra, 2016)

Type/VDD	0.4	0.5	0.6	0.7	0.8	0.9
11T (Leakage power nW)	1.2	1.35	1.55	2.55	5.1	10.25
13T (Leakage power nW)	0.096	0.586	1.102	1.986	2.952	6.102
%Improvement	92	56.59	28.90	22.11	42.11	40.46

Table 13. Few FinFET based SRAM comparison

Author Name	Technology	Name of Device	Technique Used	Special Features
Sneha et al., (Sneha et al., 2017)	45nm	7T FINFET SRAM	Supply voltage- scaling	RBL charging is not needed and Decrease in voltage supply
Yang et al., (Yang et al., 2016)	14 nm	FINFET 7 T SRAM	Near threshold voltage (NTV) operation	Efficient design solution for high performance and low energy consumption in the NTV region
Ansari et al., (Ansari et al., 2015)	20nm	FINFET 7T SRAM	NTV operation	High write, read margins and low write time
Monica et al., (Monica & Chandramohan, 2017)	16 nm	FINFET(8T SRAM)	supply voltage-floating	Improvement in read and write ability.
Yang et al., (Yatimi & Aroudam, 2018)	22nm	FINFET (single ended 9T SRAM	Near threshold (Vth) operation and yield estimation method	Minimum operating voltage of 0.3 V is achieved
Moradi et al., (Moradi & Tohidi, 2015)	22nm	FINFET(9 T SRAM)	Multi-threshold	3X lower power consumption
Oh et al., (Oh et al., 2016)	22nm	FINFET(9 T SRAM)	Power Gated 9T SRAM	Consumes less energy per read and writes operation, and smaller bit cell area.
Yadav et al., (Yadav et al., 2013)	32 nm	FINFET (10T SRAM)	Back-gate biasing and Built-in feedback mechanism	Back gate biasing and positive feedback boosts the stability.
Kaur et al., (Kaur et al., 2016)	16nm	MOSFET, FINFET (10T SRAM)	Threshold voltage technique	FINFET based memories will be used below 32nm without any SCE.
Pal et al., (Chiranjeevi & Jena, 2017)	32nm	CMOS and FINFET (10T SRAM)	Supply voltage reduction	Increase in RSNM by 20% and decrease in WSNM by 5% at 400 mV.
Farkhani et al., (Farkhani et al., 2014)	20nm	FINFET (8TSRAM)	Supply voltage	Sub threshold swing (SS) is lower in FINFET design.
Kim et al., (Kim et al., 2008)	32nm	FINFET(8 TSRAM)	Back gate voltage	Reducing the discharging activity during WRITE operation

CONCLUSION

In this survey, a number of SRAM design using FINFET technology have been reviewed. The presented analysis prove that it is better to design SRAM using FINFET because it has lower static power dissipation and delay as compare to CMOS SRAM cell and delay is also reduced in both operations. FinFETs have many advantage over the bulk MOSFET, such as FinFET developed with a process (fabrication) flow similar to conventional Silicon On Insulator (SOI) CMOS process

where as Double Gate MOSFET (DG-MOSFET) has complex fabrication process. FinFET has large packaging density compared to other DG MOSFET structures. To eliminate the SCEs, FinFET based SRAM models are presented. These models shows significant reduction in the leakage current and power dissipation when compared with conventional MOSFET based SRAM cell. Thus, this survey contributes to better understanding of the behaviour of FinFET based SRAM when low power, high speed, low leakage, and high performance are essential. Moreover, this FinFET-SRAM design is widely suited for various applications in the era of electronics such as in mobile technology, CPUs Processors, SD-RAMs etc. They are also used in different CMOS circuit low power applications. In future, Multi-Fin FinFET device can be used to enhance the driving capability of the device. This makes the era of electronics faster and reliable. However the fabrication techniques required meeting such stringent guidelines would be an issue which can also be analysed in future. Also, the transistor count may also be reduced while designing the SRAM to achieve better performance.

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