Guest Editorial Preface

Special Issue on Evolvable Hardware

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In the mid 1990s, researchers began applying Evolutionary Algorithms (EAs) - a class of powerful search algorithms inspired by the process of natural selection - on a kind of computer chip that could dynamically alter the functionality and physical connections of its circuits. This combination of EAs with programmable electronics - Field Programmable Gate Arrays (FPGAs) & Field Programmable Analogue Arrays (FPAAs) to give but two examples - spawned a new field called Evolvable Hardware (EH).

Since that time, the EH field has expanded beyond the use of EAs on simple electronic devices to encompass many different combinations of EAs and other biologically inspired algorithms (BIAs) with various physical devices (or simulations of physical devices). Present research in the field of EH can be split into the two related areas of Evolvable Hardware Design and Adaptive Hardware.

Evolvable Hardware Design is the use of EAs and BIAs for creating physical devices and designs. Examples of where this approach has had some success include analogue and digital electronics, antennas, MEMS chips, optical systems, as well as quantum circuits.

Adaptive Hardware, as the name suggests, uses EAs and BIAs to endow physical systems with some adaptive characteristics, taking the view that these are required to construct more robust components and systems to allow them to continue to operate successfully in a changing environment. For example, a circuit on an FPGA that "evolves" to heal from radiation damage or an FPAA that can change its function as operational requirements change.

The International Conference on Evolvable Systems (ICES) has been held without interruption since 1995 and has risen to become the leading conference in the field of evolvable hardware and systems. Some of the topics covered at ICES included: evolutionary hardware design, intrinsic and extrinsic evolution, on-line hardware evolution, evolutionary robotics, self-repairing and fault tolerant systems, self-reconfigurable and adaptive hardware, generative and developmental approaches, and real-world applications of evolvable hardware. In this Special Issue of the journal the authors of the four best papers were asked to prepare extended versions of their ICES papers and to include new findings and results, which they have done. To briefly introduce each of the papers.

The first paper in this issue is titled, "Investigating Power Reduction for NoC-

Based Spiking Neural Network Platforms Using Channel Encoding" by Neil McDonnell, Snaider Carrillo, Jim Harkin, and Liam McDaid, University of Ulster, UK. The paper addresses the bio-inspired paradigm of spiking neural networks and their implementation on network-on-chip devices. In particular network-on-chip (NoC) routers provide the scalable interconnection fabric for the mixed signal spiking neural network (SNNs) architecture based around the EMBRACE architecture. NoCs are known to provide a good trade-off between scalability, throughput and power consumption. Recent focus has been placed on exploring serial data links between NoC routers in order to improve signal integrity in the communication channel as clock speeds increase. However, moving streams of data between the parallel path of the internal router and external serial-channel links between them consumes additional power. Encoding the data streams to minimise switching activity in the serial links is an effective method of reducing the additional power dissipation. However, determining in real-time the correct streams to encode with minimal hardware overhead becomes an important issue particularly for large scale SNN hardware. This paper proposes a novel low area and power decision circuit for NoC channel encoding which identifies packets for encoding. It also extends the existing SILENT encoders/decoders to further minimise power consumption and demonstrates the power performance savings of the decision circuit and modified (en)decoders using example test traffic with the EMBRACE NoC router.

The next article, "Compensating Resource Fluctuations by Means of Evolvable Hardware: The Run-Time Reconfigurable Functional Unit Row Classifier Architecture,"is by Paul Kaufmann, Kyrre Glette, Marco Platzner, and Jim Torresen, University of Paderborn, Germany, and University of Oslo, Norway. The evolvable hardware (EHW) paradigm facilitates the construction of autonomous systems that can adapt to environmental changes and the degradation of computational resources available. Extending the EHW principle to architectural adaptation, the authors study the capability of evolvable hardware classifiers to adapt to intentional run-time fluctuations of the available resources, i.e., chip area, in this work. To that end, the work leverages the Functional Unit Row (FUR) architecture, a coarse-grained reconfigurable classifier, and applies it to two medical benchmarks, the Pima and Thyroid data sets from the UCI Machine Learning Repository. While quick recovery from architectural changes has already been demonstrated for the FUR architecture, in this work the authors introduce two reconfiguration schemes helping to reduce the magnitude of degradation after architectural reconfiguration.

The third article is titled, "Automatic Machine Code Generation for a Transport Triggered Architecture using Cartesian Genetic Programming", and is by James Alfred Walker, Yang Liu, Gianluca Tempesti, Jon Timmis, and Andy M. Tyrrell, University of York, UK. Transport triggered architectures are used for implementing bio-inspired systems due to their simplicity, modularity and fault-tolerance. However, producing efficient, optimised machine code for such architectures is an extremely difficult task, as the computational complexity has moved from the hardware-level to the software-level. This paper presents the application of Cartesian Genetic Programming to the evolution of machine code for a simple implementation of a transport triggered architecture. The effectiveness of the algorithm is demonstrated by evolving machine code for a 4-bit multiplier with three different levels of parallelism. The results show that 100% successful solutions were found by CGP and by further optimising the size of the solutions, it is possible to find efficient implementations of the 4-bit multiplier. The authors further enhance the system with the use of loops within the CGP function. These results show that the use of a loop function did not significantly affect the performance of the CGP algorithm but a reduction of up to 55% in the solution size was observed, which could have the potential to be classed as "human competitive."

The last paper is "Multi-View Human Body

Pose Estimation with CUDA-PSO" by L. Mussi, S. Ivekovic, Y. S. G. Nashed, and S. Cagnoni, University of Parma, Italy, and University of Strathclyde, UK. In this paper the authors formulate the body pose estimation problem as a multi-dimensional nonlinear optimization, suitable to be solved approximately by a meta-heuristic, specifically particle swarm optimization (PSO). Starting from multi-view video sequences acquired in a studio environment, a full skeletal configuration of the human body is retrieved. The authors use a generic surface sub-divided 3D model to generate solutions for the optimization problem. They then use a PSO to look for the best match between the silhouettes generated by the projection of the model in a candidate pose and the silhouettes extracted from the original video sequence. The optimization method, in this case PSO, is run in parallel on the Graphics Processing Unit (GPU) implemented within the nVidia CUDA™ architecture. The authors compare the results obtained by different configurations of the camera setup, fitness function, and PSO neighborhood topologies.

We hope you enjoy reading these papers as much as we enjoyed working on them and if this has caught your imagination, you might like to attend a future ICES event (the next one will be in 2013 in Singapore).

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Andy M. Tyrrell received a 1st class honours degree in 1982 and a PhD in 1985, both in Electrical and Electronic Engineering. He joined the Electronics Department at York University in April 1990, he was promoted to the Chair of Digital Electronics in 1998. His main research interests are in the design of biologically-inspired architectures, artificial immune systems, evolvable hardware, FPGA system design and fault tolerant design. In particular, over the last 10 years his research group at York have concentrated on bio-inspired systems including the creation of embryonic processing array, intrinsic evolvable hardware systems and the immunotronics hardware architecture. He is Head of the Intelligent Systems research group at York. He was General Programme Chair for ICES 2003 and CEC 2009 and Programme Chair for IPCAT2005. He has published over 260 papers in these areas, and has attracted funds in excess of £6M. He is a senior member of the IEEE, and a Fellow of the IET.

Gianluca Tempesti received a BSE in electrical engineering from Princeton University in 1991 and a MSE in computer science and engineering from the University of Michigan at Ann Arbor in 1993. In 1998 he received a PhD from the Ecole Polytechnique Federale de Lausanne (EPFL), Switzerland with a thesis on the design of fault-tolerant bio-inspired FPGAs. In 2003 he was granted a young professorship award from the Swiss National Science Foundation (FNS). He joined the Department of Electronics at the UY as a Reader in 2006. His research interests include bio-inspired digital hardware, built-in self-test and self-repair, programmable logic, and cellular automata, and he is author of over 75 articles in these areas. He was program chair of the Von Neumann Day (Lausanne, 1997), and program co-chair of the 6th International Conference on Evolvable Systems (Barcelona, Sept. 2005), as well as member of the program and scientific committees of several international conferences.